REMARKS

Claims 1-22 are pending in this application, of which claims 17 - 20 have been withdrawn from consideration. By this Preliminary Amendment, claims 1 and 21 have been amended. No new claims have been added.

Significant structural arrangements of the Applicants' claimed invention with regard to claims 1 and 21, as amended, now include forming a first opening for electrically connecting one of the couple of impurity diffusion layers and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film;

forming a metal film on the second insulating film for electrically connecting the one of the couple of impurity diffusion layers via the first opening and the upper electrode via the second opening; . . .

forming a third opening for electrically connecting to the other of the couple of impurity diffusion layers, by etching a part of the third insulating film; and

forming a wiring electrically connecting to the other of the couple of impurity diffusion layers, the wiring composed from different material from the local interconnection.

That is, in the present claimed invention, as amended, the impurity diffusion layer is formed by a couple of impurity diffusion layers, wherein the local interconnection is electrically connected to one of the couple of impurity diffusion layers, and the wiring is electrically connected to the other of the couple of impurity diffusion layers. Moreover, the wiring is composed from a different material than the material of the local interconnection.

Thus, the local interconnection which connects to one of the couple of impurity diffusion layers and is formed to cover the capacitor can give priority to preventing capacitor degradation by reduction gas. Further, the wiring which is connected to the other of the couple of impurity diffusion layers and whose material is different from the local interconnection can give priority to a higher conductivity than a reduction prevention action.

For example, as described in Fig. 1G, the local interconnection 9a(TiN) is electrically connected to one 3d of the impurity diffusion layers (3s,3d), and the second wiring 13 (multiplayer including Al) is electrically connected to the other 3s of impurity diffusion layers (3s, 3d). Thus, as described in claims 2 and 3, in the case that a TiN layer as the local interconnection9a is applied, the TiN layer is superior as a reduction prevention layer than an Al layer (second wiring 13), and, since a fusing current of the TiN layer is higher than that of the Al layer, the TiN layer can be used with a thin thickness unlike the Al layer.

Thus, in the case of conduction between a short distance (local interconnection and the like), since a wiring resistance does not become a problem, the TiN local interconnection having a thin thickness can be used. In this matter, since the local interconnection having a thin thickness as a reduction prevention layer can be used, the step of planarization is not necessary and a low cost process is constructed.

In contrast, in **Mochizuki**, wiring (al layer 22/TiN layer 11' etc.) composed from the same material is respectively connected to a couple of impurity diffusion layers 33,34. Since priority is given only to the high conductivity of wiring, diffusion of the reduction gas to the capacitor cannot be prevented completely. Moreover, since the step of planarization of the circumference of the capacitor is needed, the process becomes complicated.

Also, in **Watanabe** wirings 15,17 composed from the same material (Al-Si) are respectively connected to a couple impurity diffusion layers 3,4. And, in **Zafer**, wirings 42 composed from the same material (Al-Cu) are respectively connected to a couple impurity diffusion layer 204.

As above explanation, features of amended claims 1 and 21 are completely different from the cited documents. That is, the cited documents do not describe that the material is changed between the local interconnection connected to one of impurity diffusion layers and the wiring connected to the other of impurity diffusion layers, wherein the local interconnection is a reduction preventing layer of the capacitor and the local interconnection is formed to cover the entire portion above the capacitor.

In view of the aforementioned amendments and accompanying remarks, claims 1 - 22, as amended, are in condition for examination, which action, at an early date, is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosure: Version With Markings To Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims1 and 21 have been amended as follows:

1. (Thrice Amended) A method of manufacturing a semiconductor device comprising the steps of :

forming [an] a couple of impurity diffusion layers in a semiconductor substrate;

forming a first insulating film covering the semiconductor substrate;

forming a lower electrode of a capacitor on the first insulating film;

forming an oxide dielectric film of the capacitor on the lower electrode;

forming an upper electrode of the capacitor on the oxide dielectric film;

forming a second insulating film for covering the capacitor;

forming a first opening for electrically connecting one of the couple of [the] impurity diffusion layers and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film;

forming a continuous metal film on the second insulating film for electrically connecting [electrically] the one of the couple of [the] impurity diffusion layers via the first opening and the upper electrode via the second opening;

forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, in a range which passes through the first opening and the second opening, by patterning the metal film; [and]

forming a third insulating film for covering the local interconnection;

forming a third opening for electrically connecting to the other of the couple of impurity diffusion layers, by etching a part of the first, second and third insulating films; and

forming a wiring electrically connecting to the other of the couple of impurity diffusion layers, the wiring composed from different material from the local interconnection.

21. (Thrice Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming [an] a couple of impurity diffusion layers in a semiconductor substrate;

forming a first insulating film covering the semiconductor substrate;

forming a lower electrode of a capacitor on the first insulating film;

forming an oxide dielectric film of the capacitor on the lower electrode;

forming an upper electrode of the capacitor on the oxide dielectric film;

forming a second insulating film for covering the capacitor;

forming a first opening for electrically connecting one of the couple of [the] impurity diffusion layers and a second opening which exposes the upper electrode in the first and second

insulating films, by etching a part of the second insulating film and a part of the first insulating film;

forming a metal film on the second insulating film for electrically connecting [electrically] the one of the couple of [the] impurity diffusion layers via the first opening and the upper electrode via the second opening;

forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, in a range which passes through the first opening and the second opening, by patterning the metal film, wherein the local interconnection is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film; [and]

forming a third insulating film for covering the local interconnection;

forming a third opening for electrically connecting to the other of the couple of impurity diffusion layers, by etching a part of the third insulating film; and

forming a wiring electrically connecting to the other of the couple of impurity diffusion layers, the wiring composed from different material from the local interconnection.